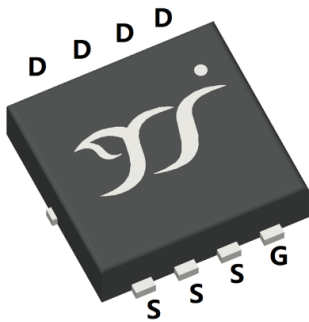
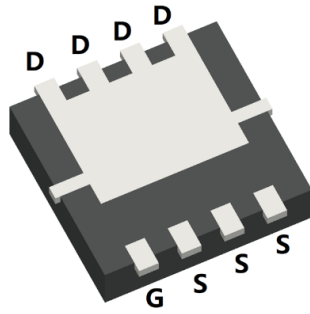


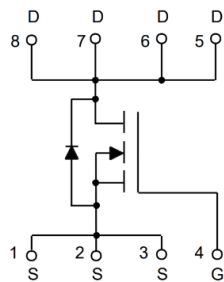
N-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View



PDFN3333-8L

Product Summary

- V_{DS} 30V
- I_D 55A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<6.5m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<12m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	12	A
	$T_A=100^\circ C$		7.5	
	$T_C=25^\circ C$		55	
	$T_C=100^\circ C$		34	
Pulsed Drain Current ^A		I_{DM}	200	A
Avalanche energy ^B		EAS	72	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	2	W
	$T_A=100^\circ C$		0.8	
	$T_C=25^\circ C$		41	
	$T_C=100^\circ C$		16	
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +150$	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	50	60	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.5	3	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ35N03A	F1	Q35N03A	5000	10000	100000	13" reel



YJQ35N03A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
		V _{DS} =30V, V _{GS} =0V, T _J =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	4.9	6.5	mΩ
		V _{GS} =4.5V, I _D =15A	-	8.7	12	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	2.5	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	55	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz	-	1045	-	pF
Output Capacitance	C _{oss}		-	180	-	
Reverse Transfer Capacitance	C _{rss}		-	155	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =20A	-	24	-	nC
Gate-Source Charge	Q _{gs}		-	5	-	
Gate-Drain Charge	Q _{gd}		-	6	-	
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us	-	0.66	-	nC
Reverse Recovery Time	t _{rr}		-	10	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =15V, I _D =20A R _{GEN} =3Ω	-	11	-	ns
Turn-on Rise Time	t _r		-	55	-	
Turn-off Delay Time	t _{D(off)}		-	27	-	
Turn-off fall Time	t _f		-	66	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=25V, V_G=10V, R_G=25Ω, L=1mH, I_{AS}=12A.

C. P_d is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



Typical Electrical and Thermal Characteristics Diagrams

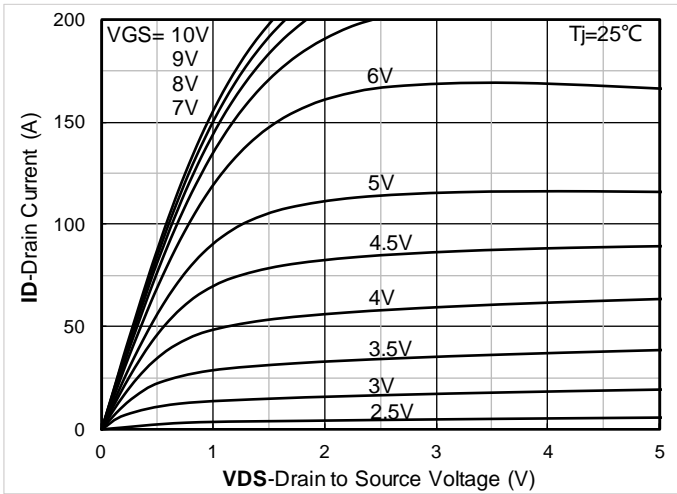


Figure 1. Output Characteristics

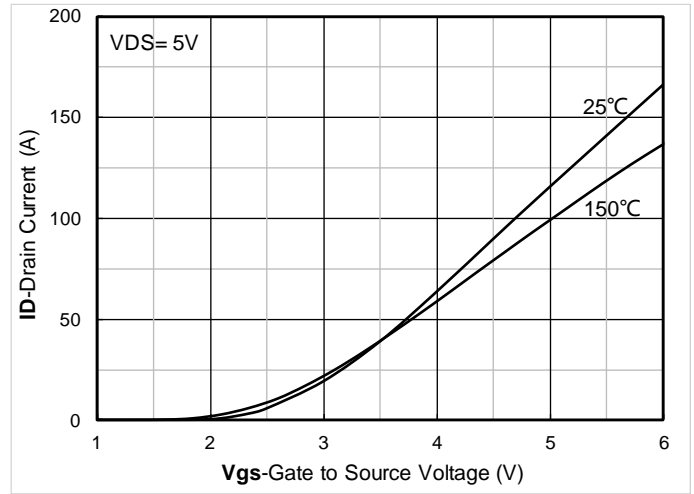


Figure 2. Transfer Characteristics

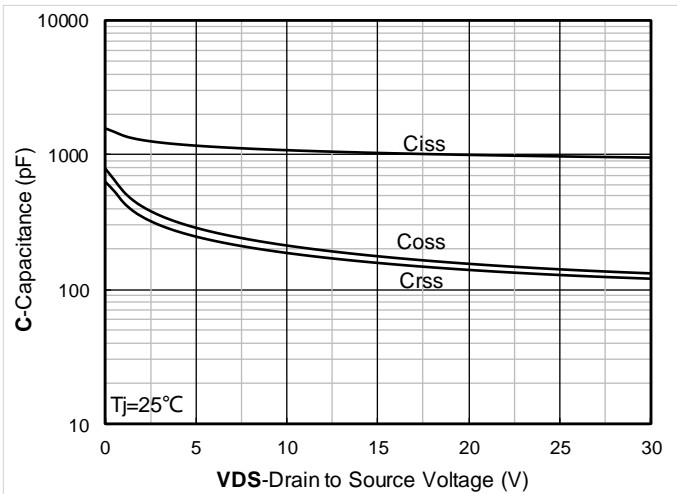


Figure 3. Capacitance Characteristics

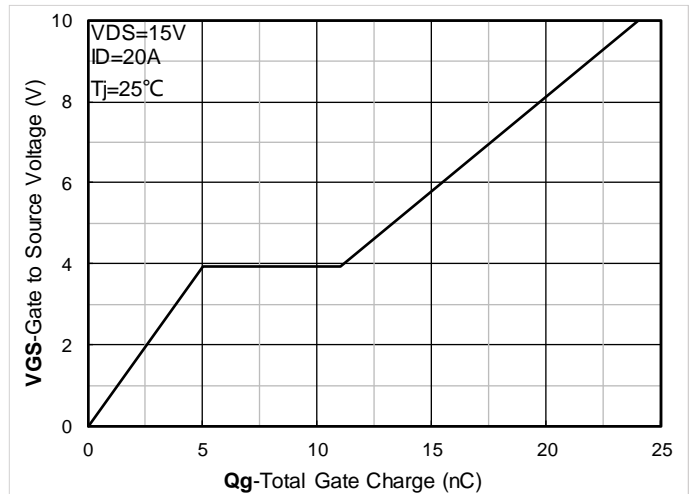


Figure 4. Gate Charge

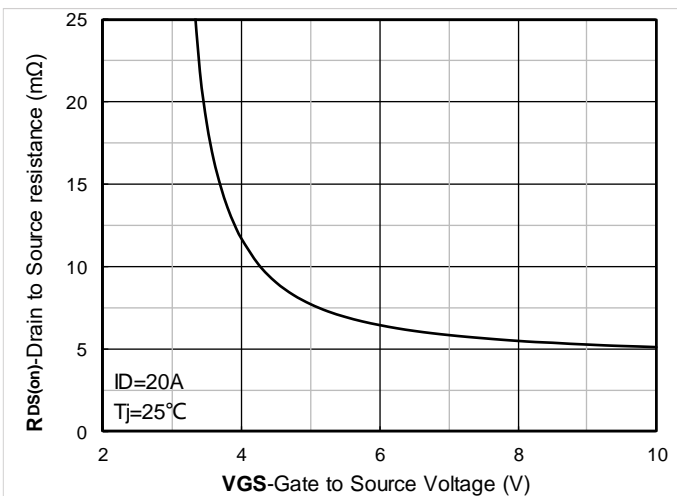


Figure 5. On-Resistance vs Gate to Source Voltage

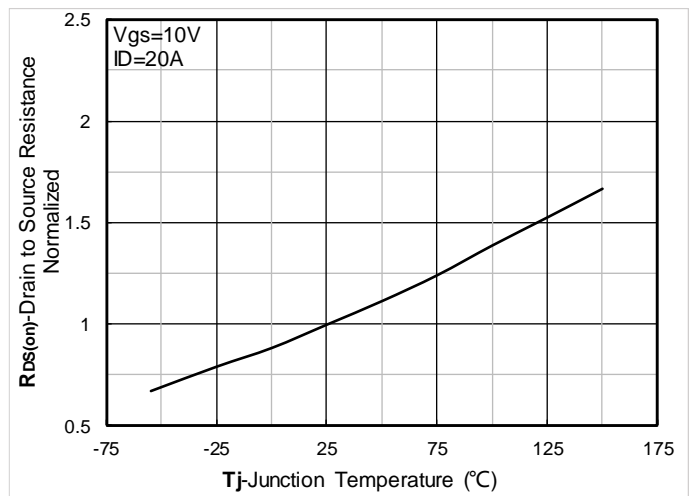


Figure 6. Normalized On-Resistance



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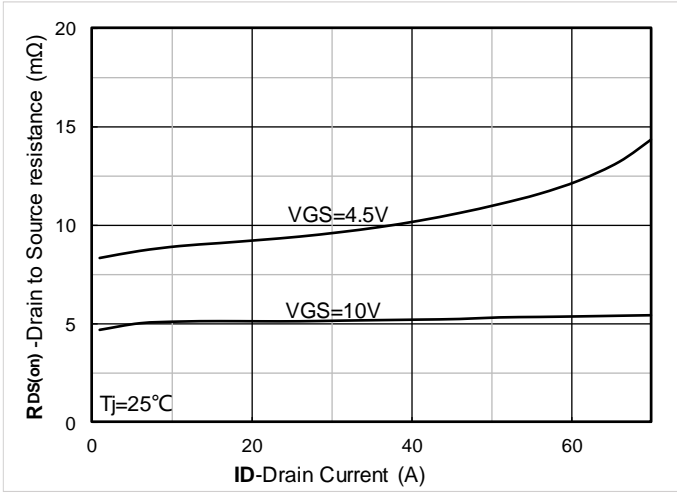


Figure 7. $R_{DS(on)}$ VS Drain Current

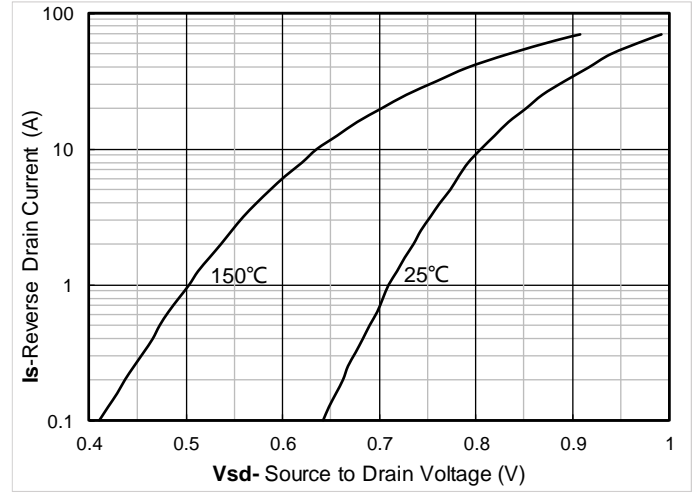


Figure 8. Forward characteristics of reverse diode

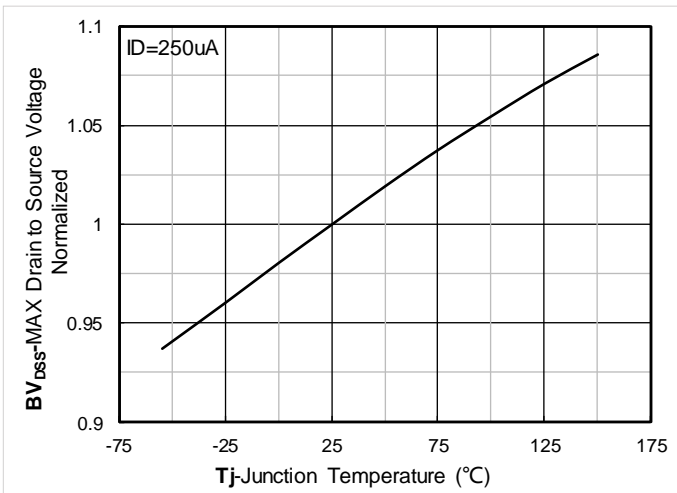


Figure 9. Normalized breakdown voltage

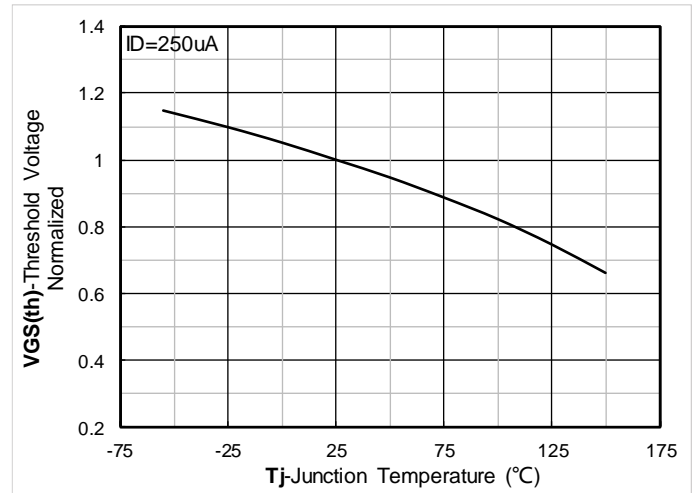


Figure 10. Normalized Threshold voltage

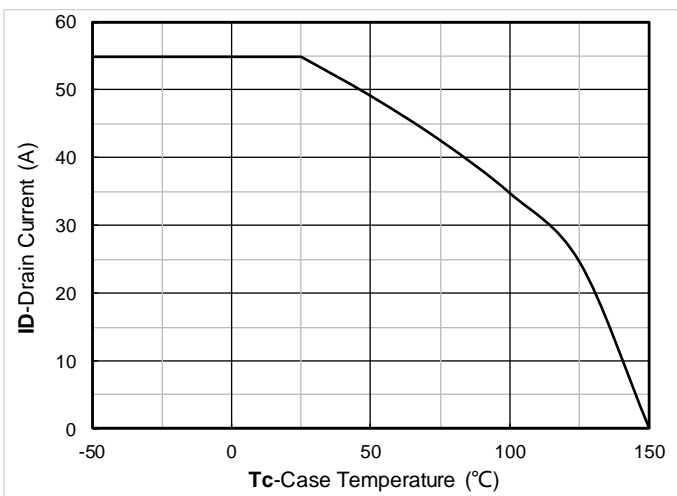


Figure 11. Current dissipation

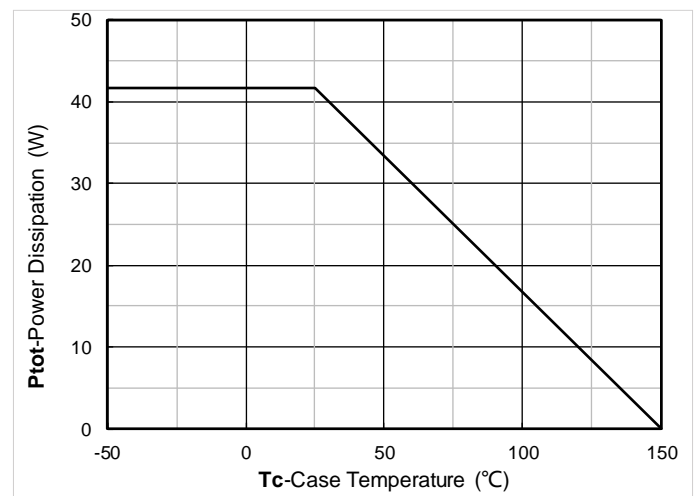


Figure 12. Power dissipation

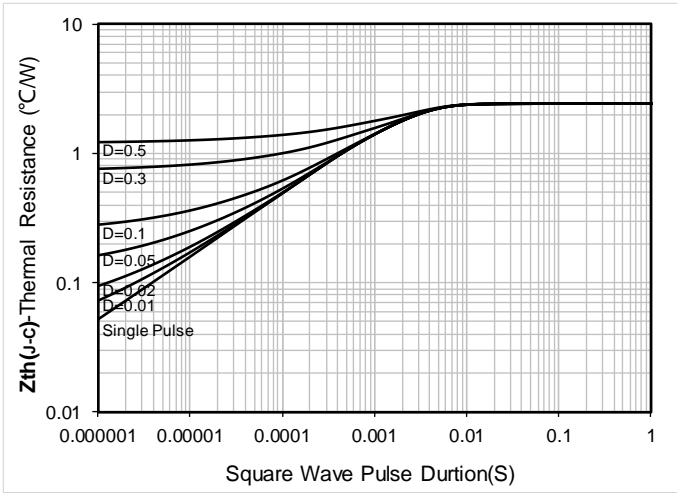


Figure 13. Maximum Transient Thermal Impedance

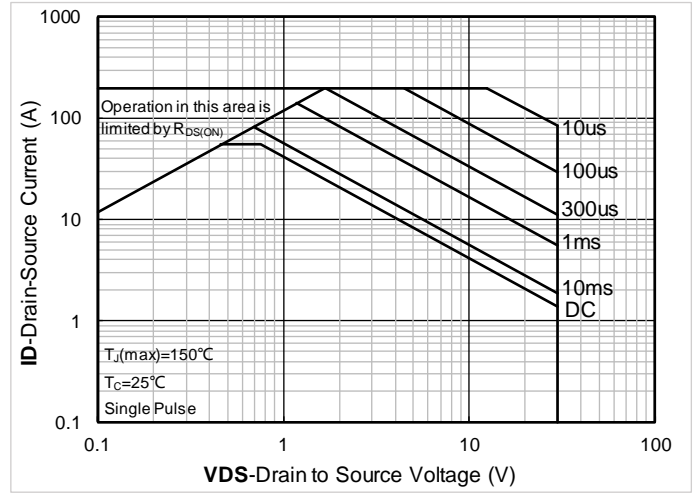


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

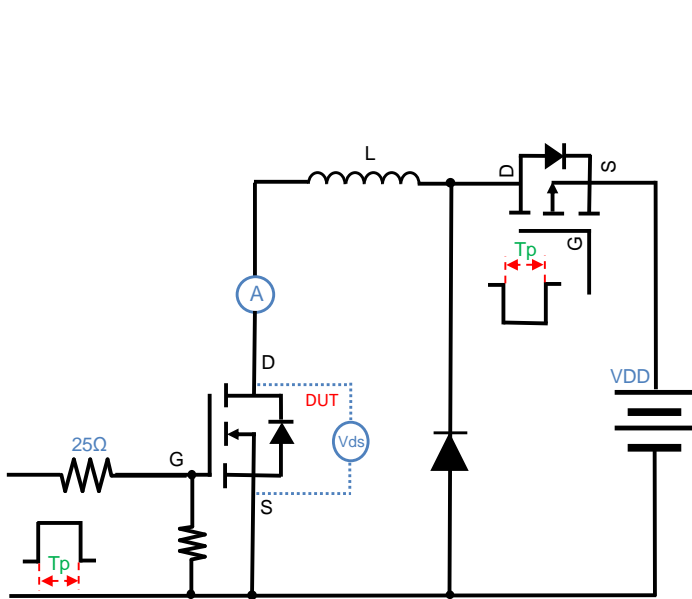
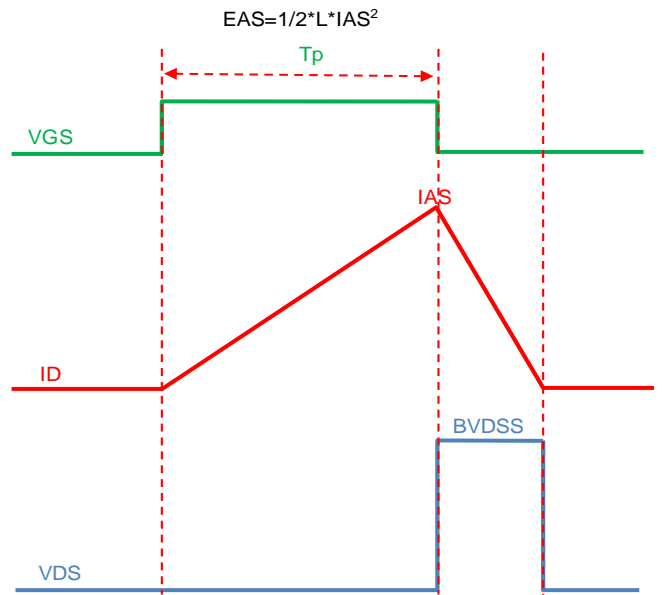


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



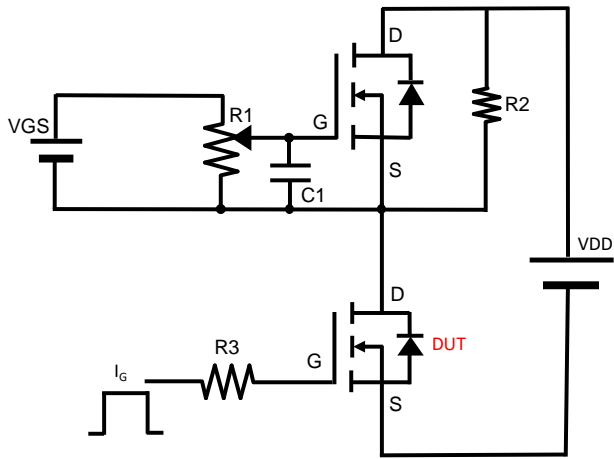


Figure B. Gate Charge Test Circuit & Waveform

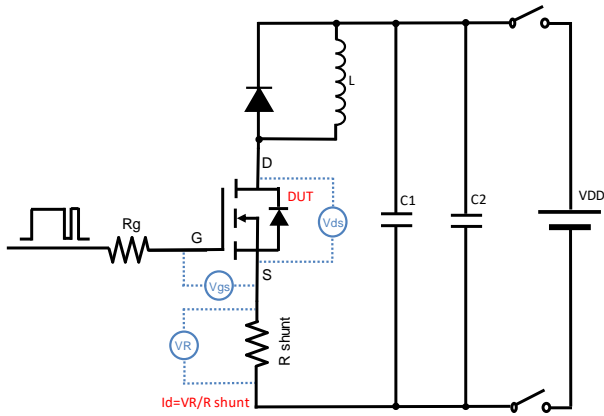


Figure C. Resistive Switching Test Circuit & Waveform

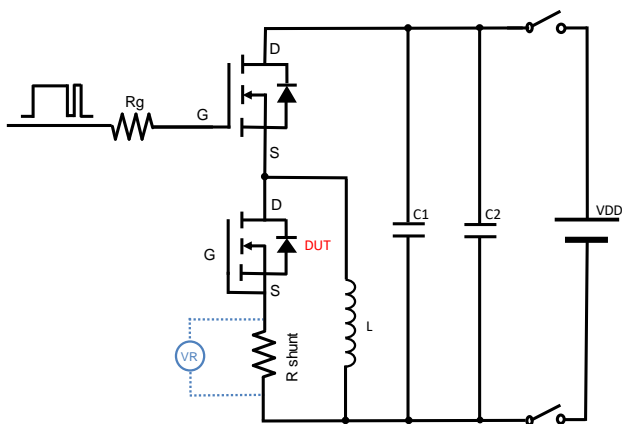
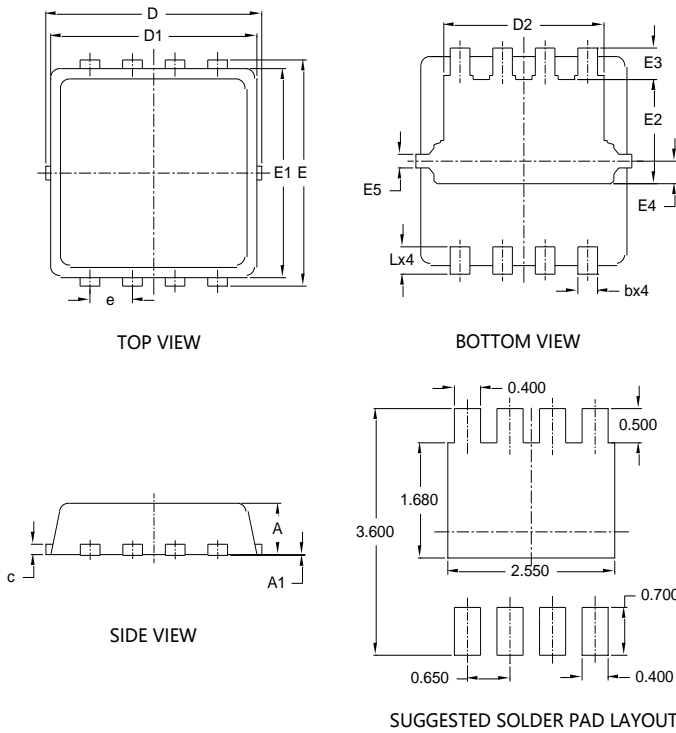


Figure D. Diode Recovery Test Circuit & Waveform



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■ PDFN3333-8L-B Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.028	0.033	0.700	0.850
A1	0.000	0.002	0.000	0.050
b	0.008	0.016	0.200	0.400
c	0.004	0.010	0.100	0.250
D	0.124	0.136	3.150	3.450
D1	0.118	0.130	3.000	3.300
D2	0.089	0.104	2.250	2.650
E	0.124	0.136	3.150	3.450
E1	0.114	0.126	2.900	3.200
E2	0.052	0.068	1.320	1.720
E3	0.011	0.026	0.280	0.650
E4	0.013 REF		0.330 REF	
E5	0.008 REF		0.200 REF	
e	0.026 BSC		0.650 BSC	
L	0.012	0.020	0.300	0.500

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

UNIT: mm



YJQ35N03A

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