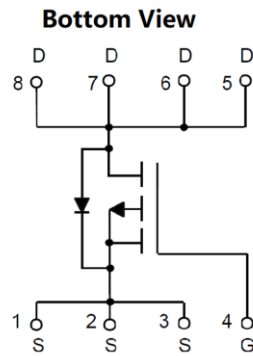
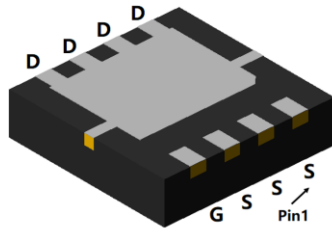
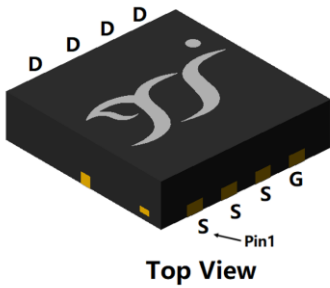


## P-Channel Enhancement Mode Field Effect Transistor



**DFN3333-8L**

### Product Summary

• $V_{DS}$	-20 V
• $I_D$	-35 A
• $R_{DS(ON)}$ ( at $V_{GS}=-4.5V$ )	<13 m $\Omega$
• $R_{DS(ON)}$ ( at $V_{GS}=-2.5V$ )	<18 m $\Omega$
• $R_{DS(ON)}$ ( at $V_{GS}=-1.8V$ )	<29 m $\Omega$
• 100% EAS Tested	

### General Description

- Trench Power LV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Battery protection
- Power management
- Load switch

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	-20	V
Gate-source Voltage		$V_{GS}$	$\pm 10$	V
Drain Current	$T_A=25^\circ C$	$I_D$	-8	A
	$T_A=100^\circ C$		-5	
	$T_C=25^\circ C$		-35	
	$T_C=100^\circ C$		-22	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	-140	A
Avalanche energy <sup>B</sup>		EAS	98	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	1.65	W
	$T_A=100^\circ C$		0.65	
	$T_C=25^\circ C$		27	
	$T_C=100^\circ C$		11	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{\theta JA}$	60	75	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	3.7	4.5	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ35P02A	F1	Q35P02A	5000	10000	100000	13" reel



# YJQ35P02A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V	-	-	-1	μA
		V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	-100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.4	-0.62	-1	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A	-	10	13	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-15A	-	13.5	18	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-10A	-	19	29	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-20A, V <sub>GS</sub> =0V	-	-	-1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	13	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	-35	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHz	-	2010	-	pF
Output Capacitance	C <sub>oss</sub>		-	270	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	240	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-17A	-	23.6	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	3.2	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	5.9	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-17A, di/dt=100A/us	-	76	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	81	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-4.5V, V <sub>DD</sub> =-10V, I <sub>D</sub> =-17A R <sub>GEN</sub> =6Ω	-	9	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	15	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	147	-	
Turn-off fall Time	t <sub>f</sub>		-	88	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>G</sub>=-5V, R<sub>G</sub>=25Ω, L=1mH, I<sub>AS</sub>=-14A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with T<sub>A</sub>=25°C.

The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



# YJQ35P02A

## Typical Electrical and Thermal Characteristics Diagrams

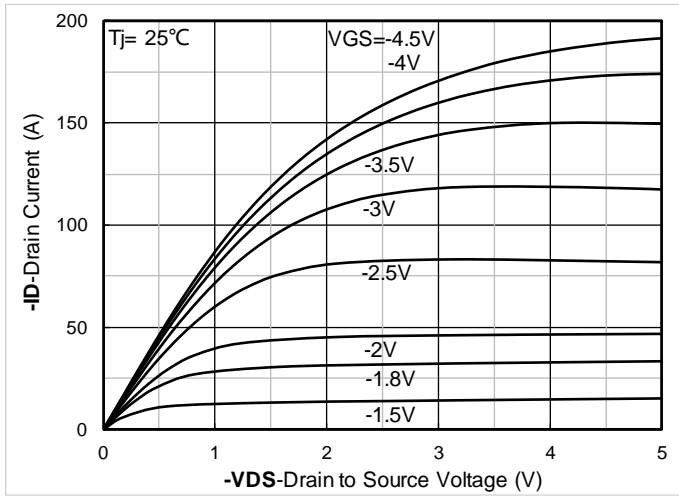


Figure 1. Output Characteristics

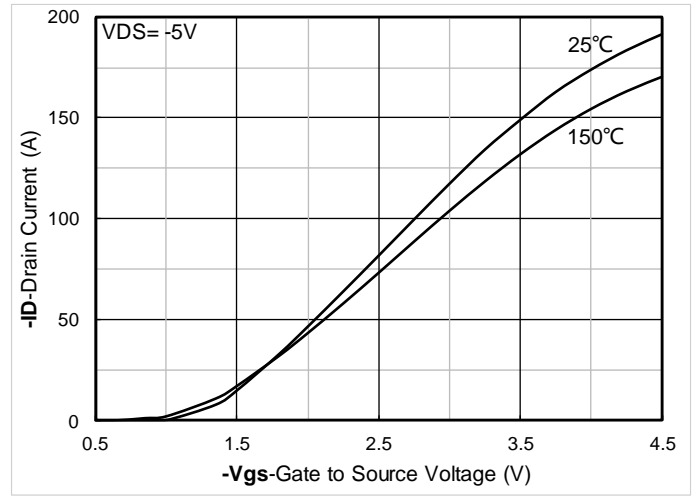


Figure 2. Transfer Characteristics

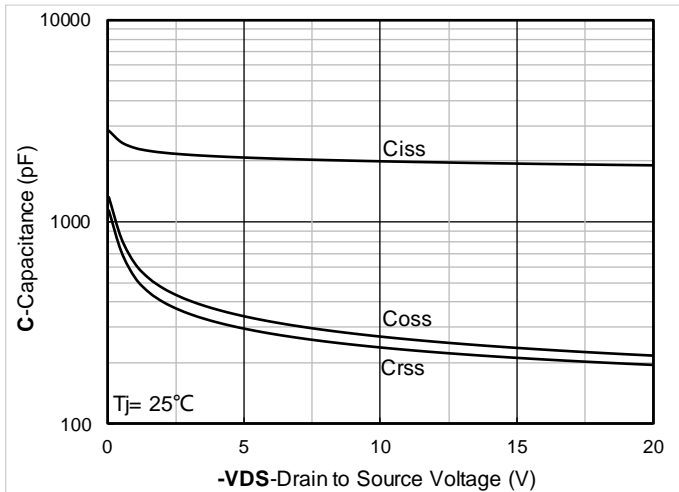


Figure 3. Capacitance Characteristics

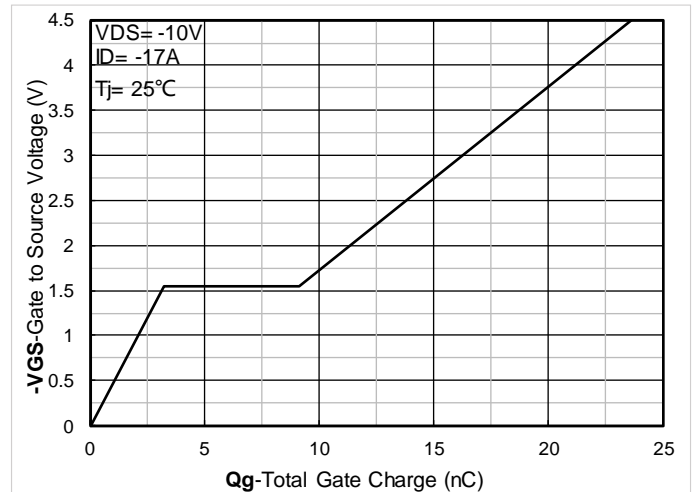


Figure 4. Gate Charge

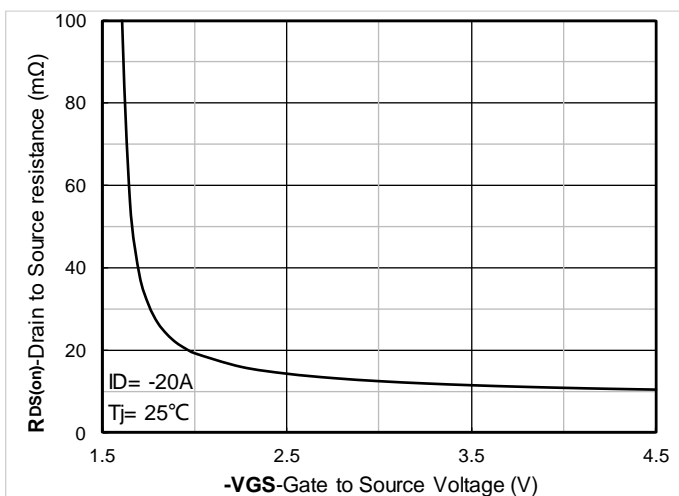


Figure 5. On-Resistance vs Gate to Source Voltage

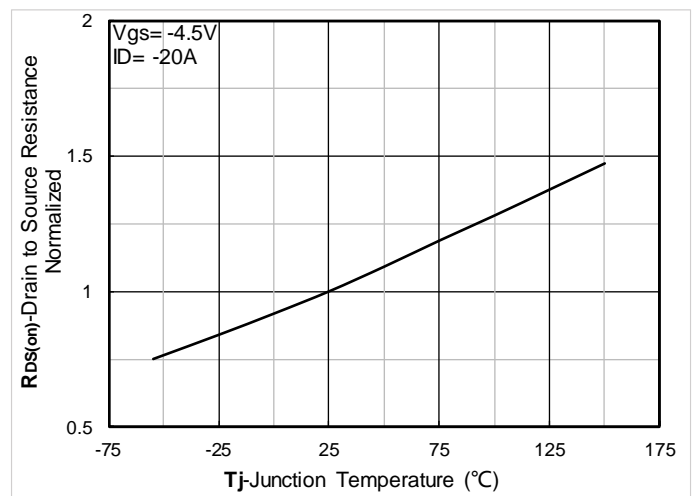


Figure 6. Normalized On-Resistance



# YJQ35P02A

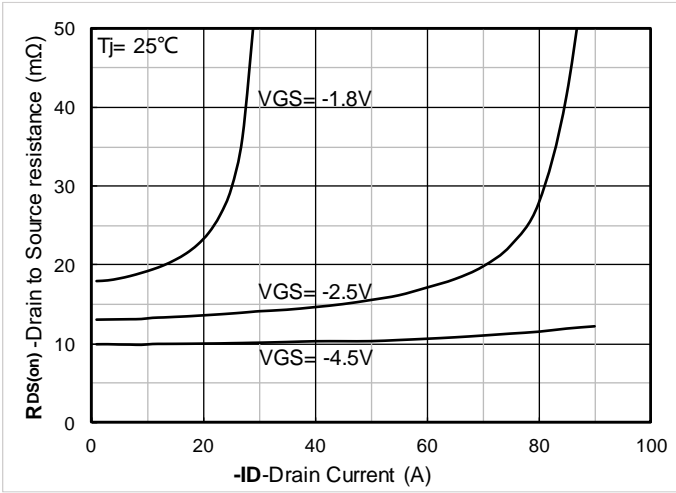


Figure 7.  $R_{DS(on)}$  VS Drain Current

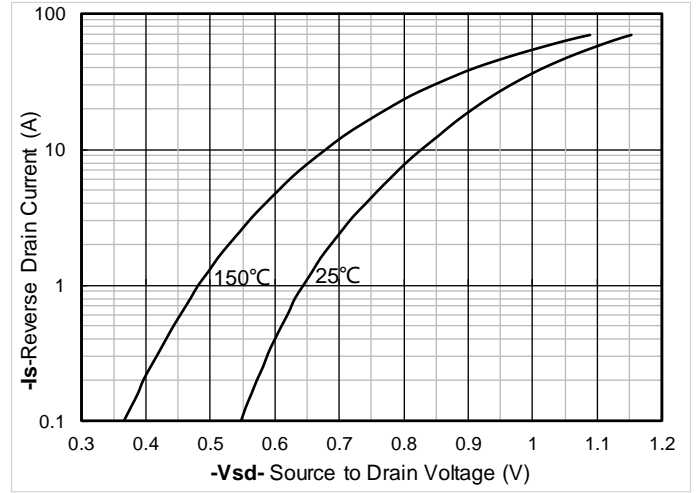


Figure 8. Forward characteristics of reverse diode

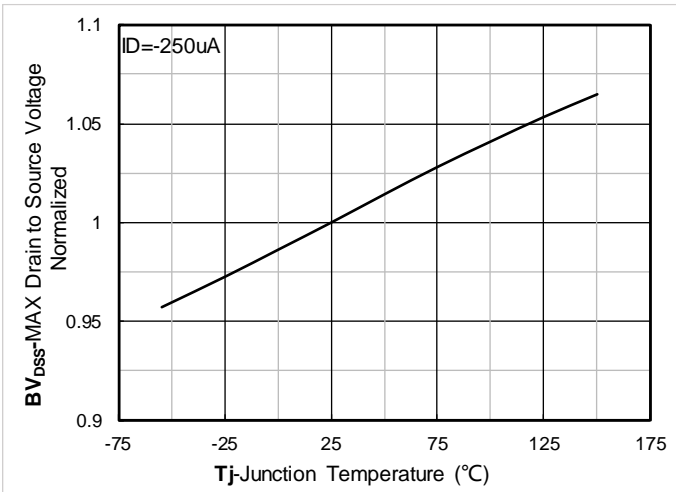


Figure 9. Normalized breakdown voltage

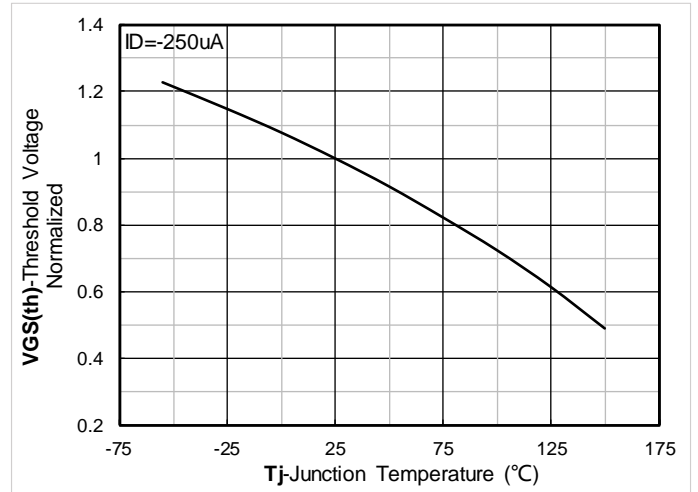


Figure 10. Normalized Threshold voltage

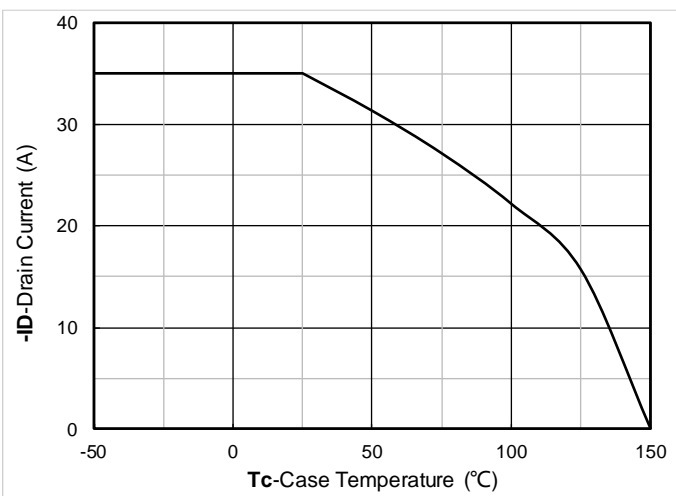


Figure 11. Current dissipation

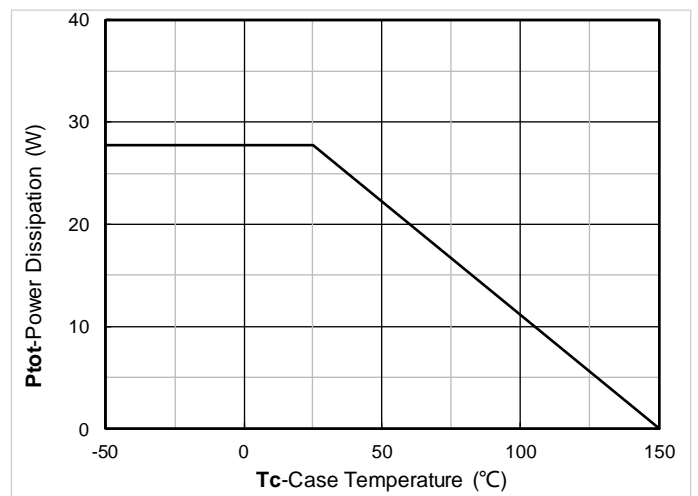


Figure 12. Power dissipation



# YJQ35P02A

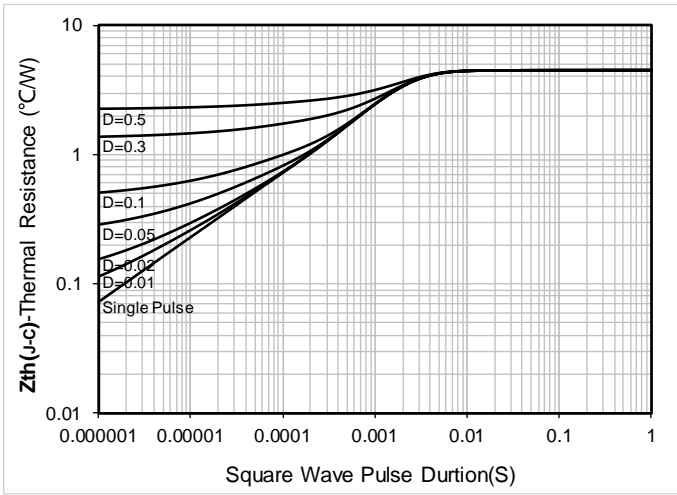


Figure 13. Maximum Transient Thermal Impedance

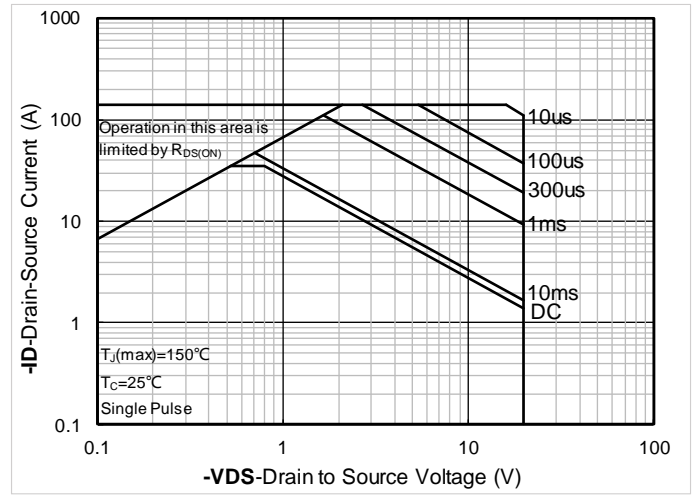
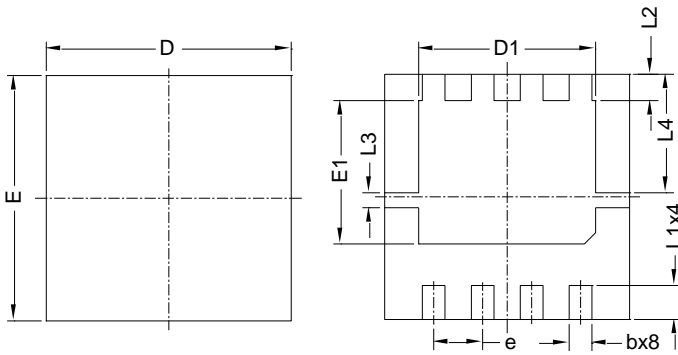


Figure 14. Safe Operation Area



# YJQ35P02A

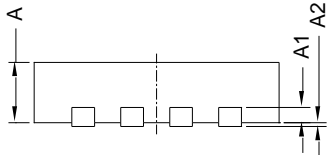
## DFN3333-8L-A-0.8MM Package information



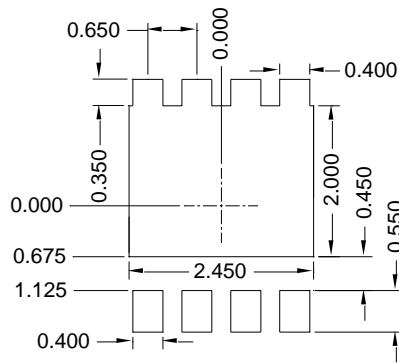
Top View  
正面视图

Bottom View  
背面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
L3	0.20 BSC		
L4	1.57 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



## YJQ35P02A

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